8XC196KC/8XC196KC20 COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

87C196KC-16 Kbytes of On-Chip OTPROM
83C196KC-16 Kbytes ROM
80C196KC-ROMless

- **16 and 20 MHz Available**
- **488 Byte Register RAM**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **Peripheral Transaction Server**
- **1.4 μs 16 x 16 Multiply (20 MHz)**
- **2.4 μs 32/16 Divide (20 MHz)**
- **Powerdown and Idle Modes**
- **Five 8-Bit I/O Ports**
- **16-Bit Watchdog Timer**
- **Extended Temperature Available**
- **Dynamically Configurable 8-Bit or 16-Bit Buswidth**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Up/Down Counter with Capture**
- **3 Pulse-Width-Modulated Outputs**
- **Four 16-Bit Software Timers**
- **8- or 10-Bit A/D Converter with Sample/Hold**
- **$\overline{HOLD}$/$\overline{HLDA}$ Bus Protocol**
- **OTPROM One-Time Programmable Version**

The 80C196KC 16-bit microcontroller is a high performance member of the MCS® 96 microcontroller family. The 80C196KC is an enhanced 80C196KB device with 488 bytes RAM, 16 and 20 MHz operation and an optional 16 Kbytes of ROM/OTPROM. Intel's CHMOS III process provides a high performance processor along with low power consumption.

The 87C196KC is an 80C196KC with 16 Kbytes on-chip OTPROM. The 83C196KC is an 80C196KC with 16 Kbytes factory programmed ROM. In this document, the 80C196KC will refer to all products unless otherwise stated.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended (Express) temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

See the Packaging information for extended temperature designators.

July 2004 **Order Number:270942-006**

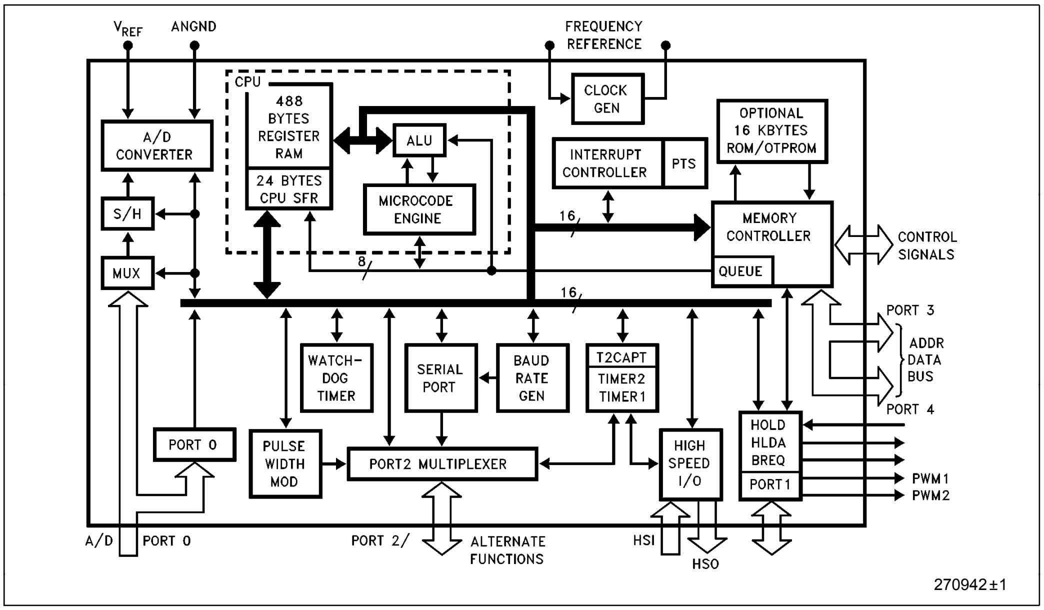
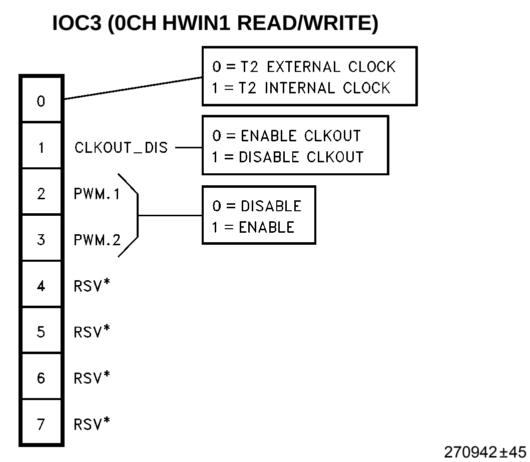


Figure 1. 8XC196KC Block Diagram

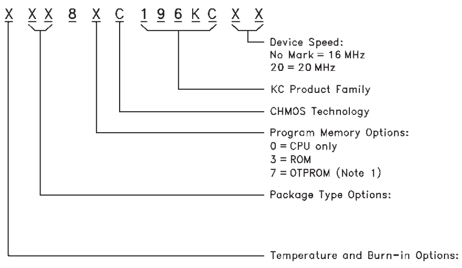


NOTE:
*RSV-Reserved bits must be = 0

Figure 2. 8XC196KC New SFR Bit (CLKOUT Disable)

PROCESS INFORMATION

This device is manufactured on PX29.5 or PX29.9, a CHMOS III process. Additional process and reliability information is available in the Intel® Quality *System Handbook:*
http://developer.intel.com/design/quality/quality.htm



270942–43

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196KC Family Nomenclature

Table 1. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13 °C/W
QFP	55°C/W	16 °C/W
SQFP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 2. 8XC196KC Memory Map

Description	Address
External Memory or I/O	0FFFFH 06000H
Internal ROM/OTPROM or External Memory (Determined by $\overline{EA}$)	5FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/OTPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H. (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4	1FFFH 1FFEH
External Memory	1FFDH 0200H
488 Bytes Register RAM (Note 1)	01FFH 0018H
CPU SFR's (Notes 1, 3, 4)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 01FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC User's manual for SFR descriptions.
5. WARNING: Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

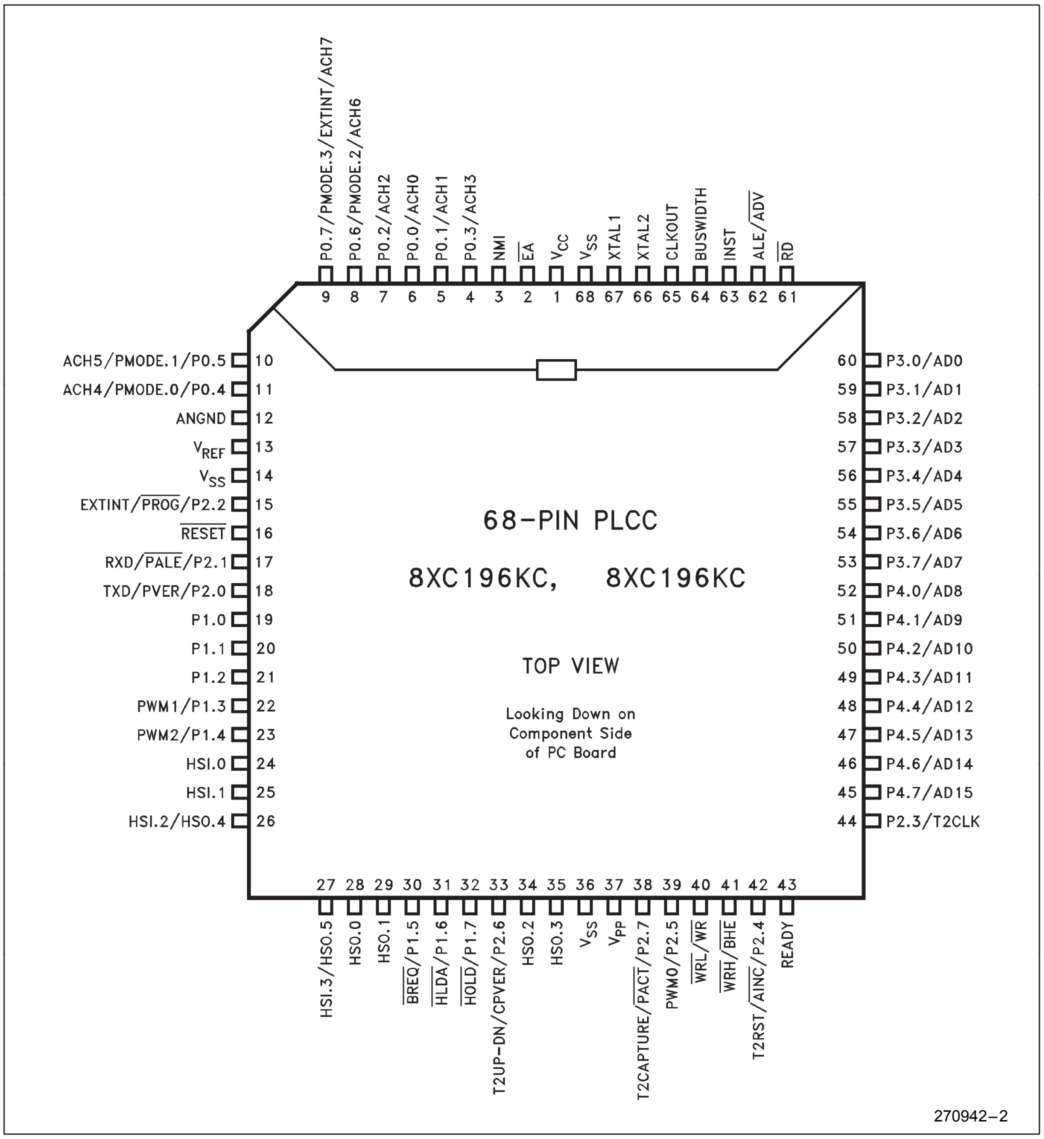


Figure 4. 68-Lead PLCC Package

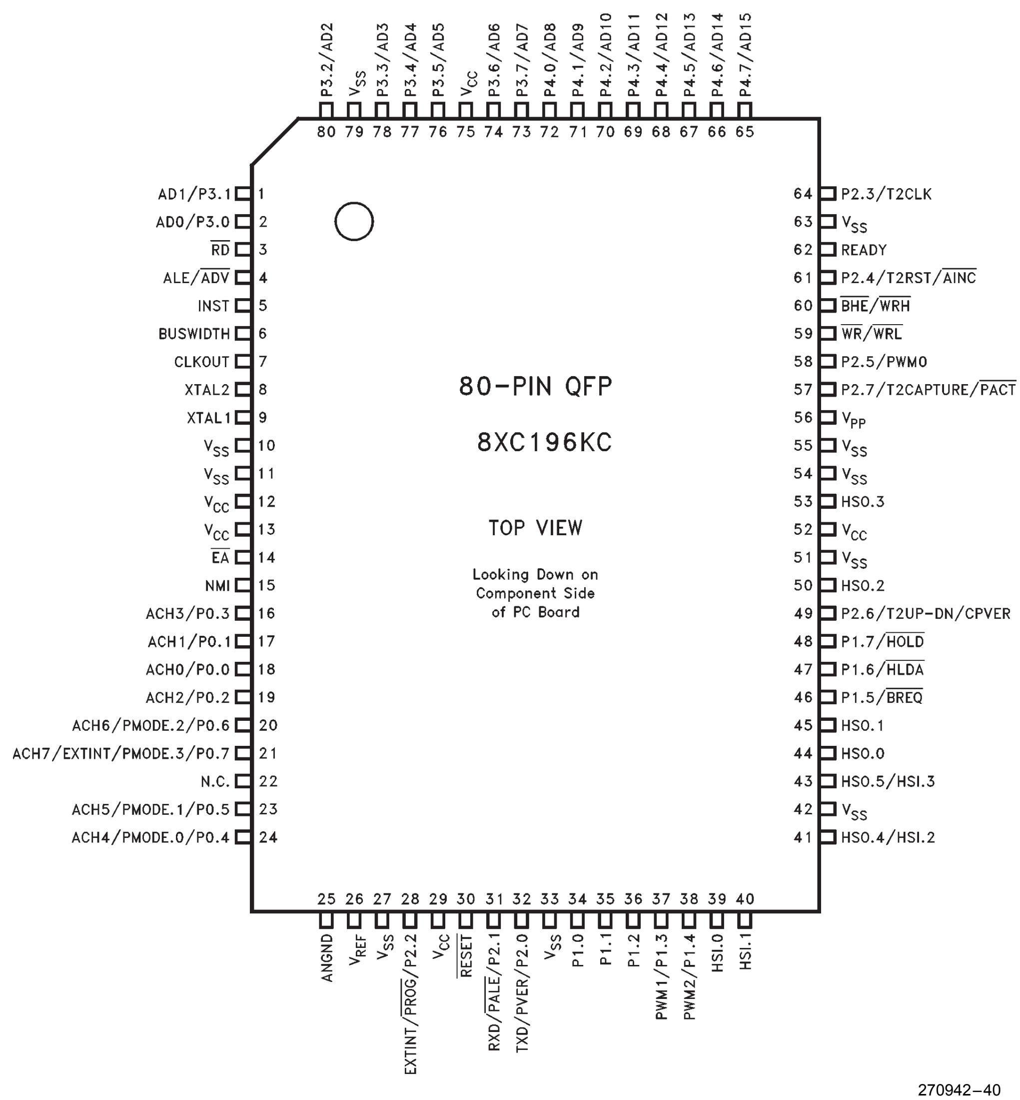


Figure 5. 8XC196KC 80-Pin QFP Package

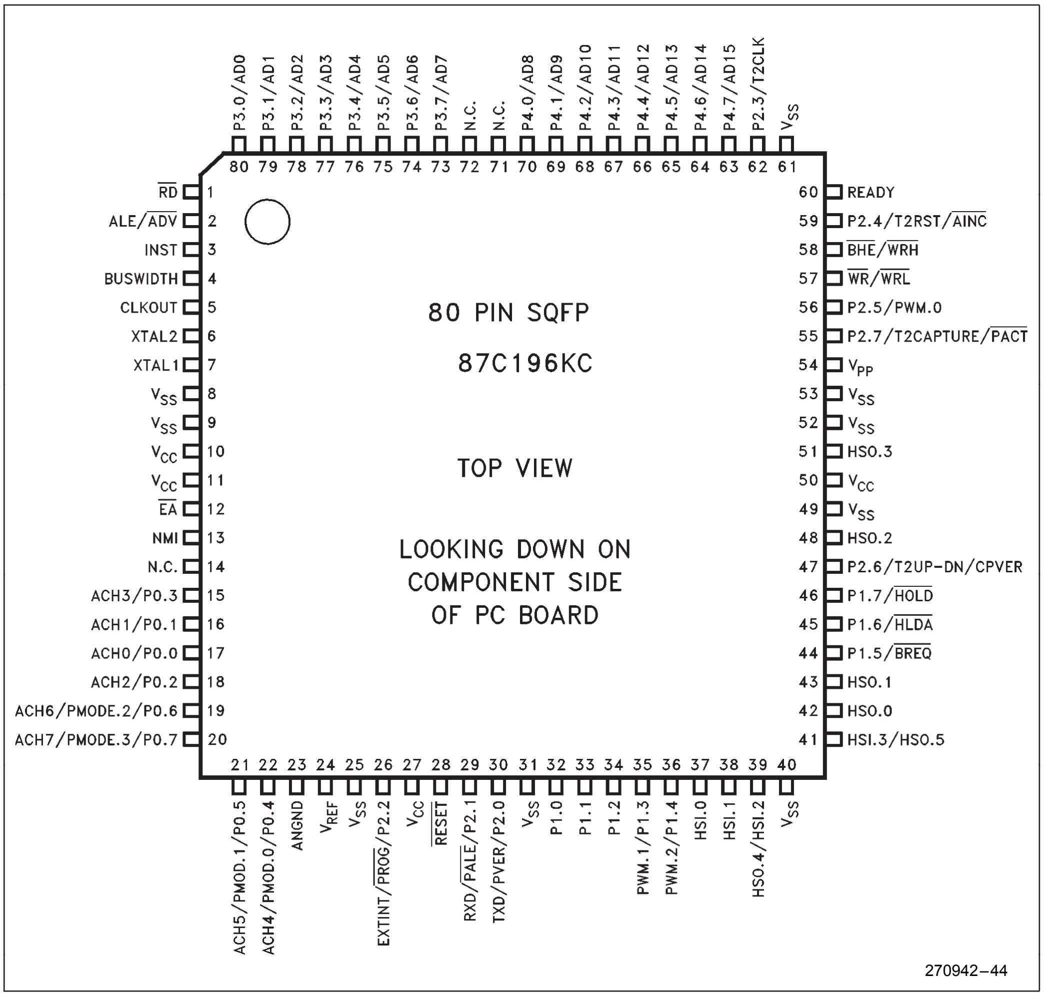


Figure 6. 80-Pin SQFP Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. This pin also supplies the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{RESET}$	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip ROM/E PROM. $\overline{EA}$ equal to low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KC. Pins 2.6 and 2.7 are quasi-bidirectional.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
CPVER	Cummulative Program Output Verification. Pin is high if all locations have programmed correctly since entering a programming mode.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programmig Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
$\overline{\text{AINC}}$	Auto Increment. Active low input signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ELECTRICAL CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ....-55° to +125°C

Storage Temperature ....-65° to +150°C

Voltage On Any Pin to V_{SS} ....-0.5V to +7.0V(1)

Voltage from $\overline{EA}$ or
V_{PP} to V_{SS} or ANGND ....+13.00V

Power Dissipation ....1.5W(2)

NOTE:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This is a production data sheet. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING:* *Stressing the device beyond the ``Absolute Maximum Ratings'' may cause permanent damage. These are stress ratings only. Operation beyond the ``Operating Conditions'' is not recommended and extended exposure beyond the ``Operating Conditions'' may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias Extended Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} − 0.4	V_{SS} + 0.4	V(1)
F_{OSC}	Oscillator Frequency (8XC196KC)	8	16	MHz
F_{OSC}	Oscillator Frequency (8XC196KC20)	8	20	MHz

NOTE:
1. ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Over Specified Operating Conditions)

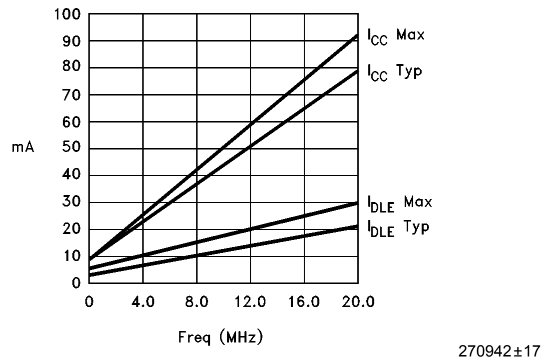
Symbol	Description	Min	Typ	Max	Units	TestConditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2		V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	300			mV	V_{CC} = 5.0V
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)			0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA

DC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	TestConditions
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10\ \mu A$ $I_{OH} = -30\ \mu A$ $I_{OH} = -60\ \mu A$
I_{OH1}	Logical 1 Output Current in Reset. on P2.0. Do not exceed this or device may enter test modes.	−0.8			mA	$V_{IH} = V_{CC} - 1.5V$
I_{IL2}	Logical 0 Input Current in Reset on P2.0. Maximum current that must be sunk by external device to ensure test mode entry.			TBD	mA	$V_{IN} = 0.45V$
I_{IH1}	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			+200	μA	$V_{IN} = V_{CC} = 2.4V$
I_{LI}	Input Leakage Current (Std. Inputs)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	$V_{IN} = 0.45V$
I_{IL1}	Ports 3 and 4 in Reset			−70	μA	$V_{IN} = 0.45V$
I_{CC}	Active Mode Current in Reset (8XC196KC)		65	75	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{CC}	Active Mode Current in Reset (8XC196KC20)		80	92	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current (8XC196KC)		17	25	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current (8XC196KC20)		21	30	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		8	15	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	$V_{CC} = 5.5V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.
3. Commercial specifications apply to express parts except where noted.
4. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
5. Standard Outputs include AD0±15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
6. Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
7. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
8. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
9. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0±AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST±CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA



I_{CC} Max = 4.13 × Frequency + 9 mA
I_{CC} Typ = 3.50 × Frequency + 9 mA
I_{IDLE} Max = 1.25 × Frequency + 5 mA
I_{IDLE} Typ = 0.88 × Frequency + 3 mA

NOTE:
Frequencies below 8 MHz are shown for reference only; no testing is performed.

Figure 7. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 80C196KC:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 68	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 68	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 22	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 45	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

AC CHARACTERISTICS (Continued)

For user over specified operating conditions.

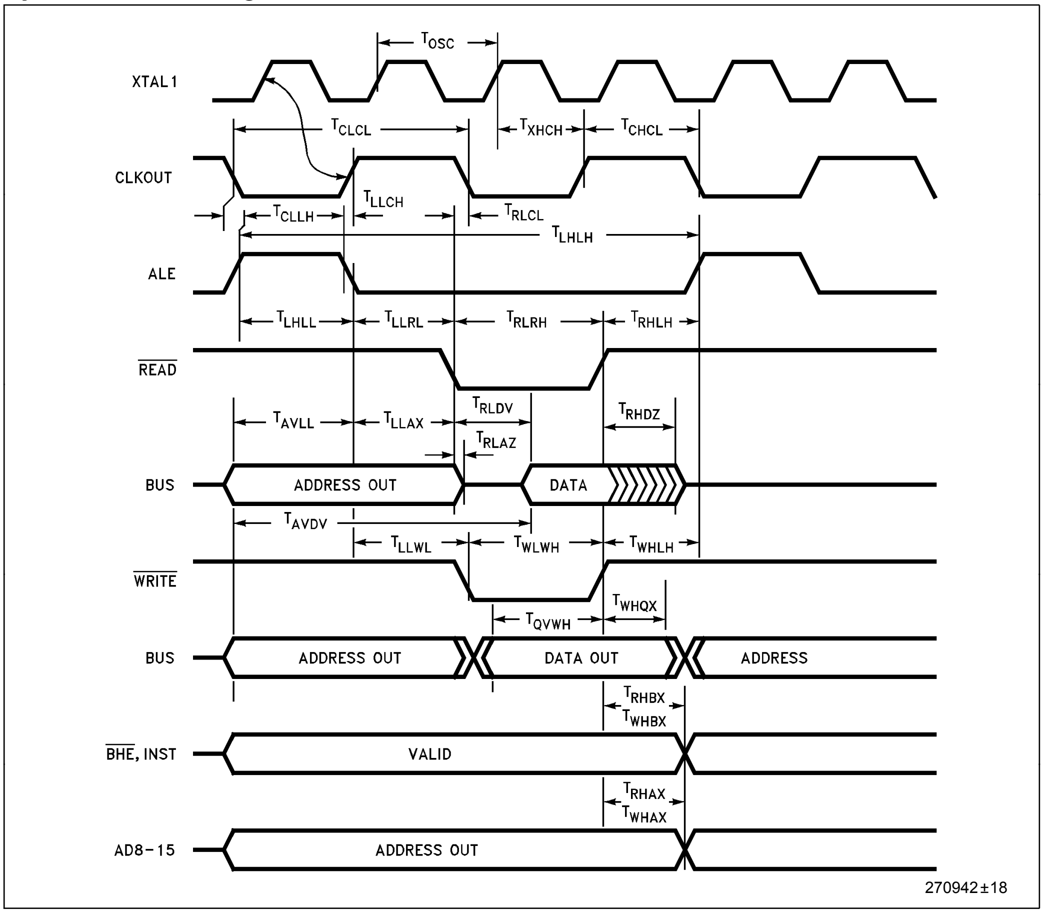
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The 80C196KC will meet these specifications:

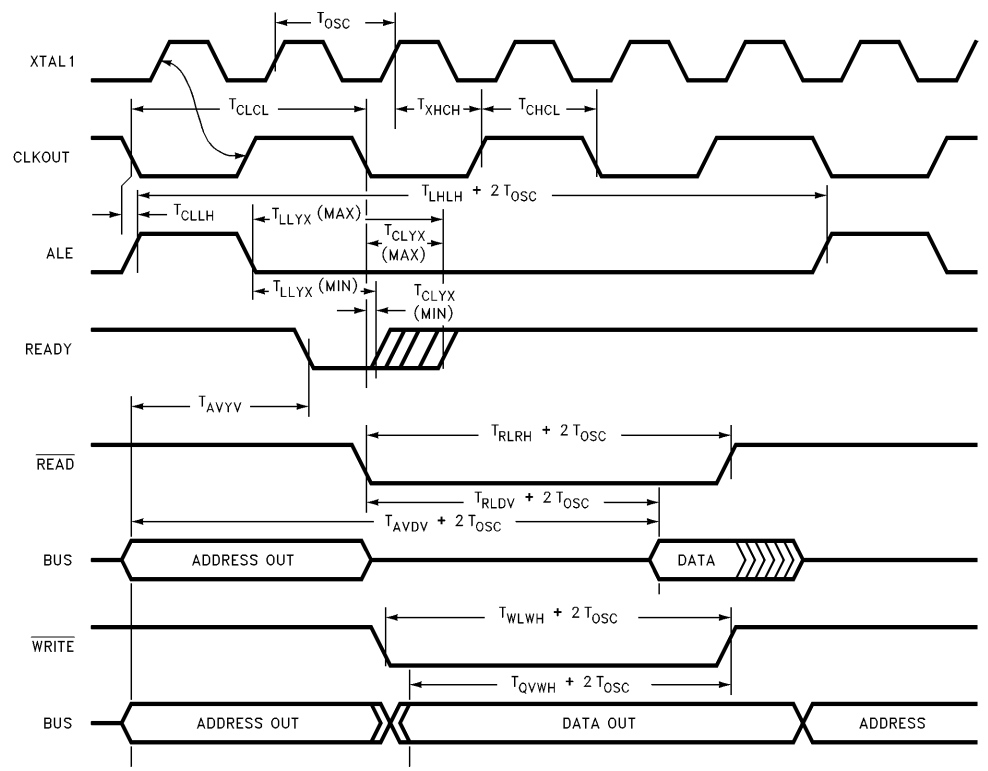
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 (**8XC196KC**)	8	16	MHz	(Note 1)
F_{XTAL}	Frequency on XTAL1 (**8XC196KC20**)	8	20	MHz	(Note 1)
T_{OSC}	I/F $_{XTAL}$ (**8XC196KC**)	62.5	125	ns	
T_{OSC}	I/F $_{XTAL}$ (**8XC196KC20**)	50	125	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	+15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 4)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 35		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 20		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8±15 HOLD after $\overline{WR}$ Rising	T_{OSC} − 30		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHAX}	AD8±15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 25		ns	(Note 3)

NOTES:
1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

System Bus Timings

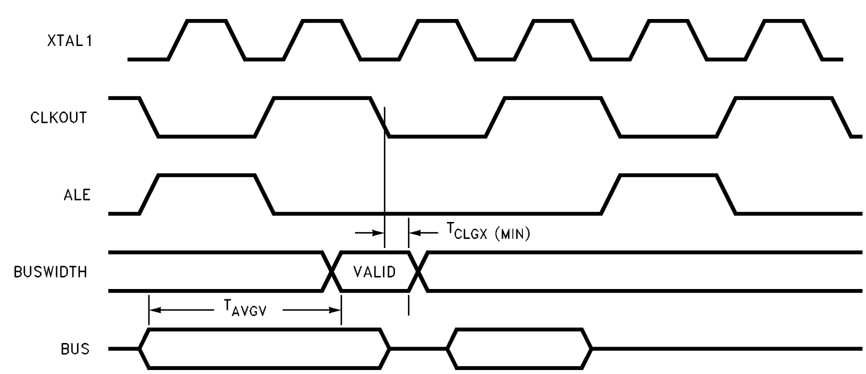


READY Timings (One Wait State)



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Buswidth Timings



270942±35

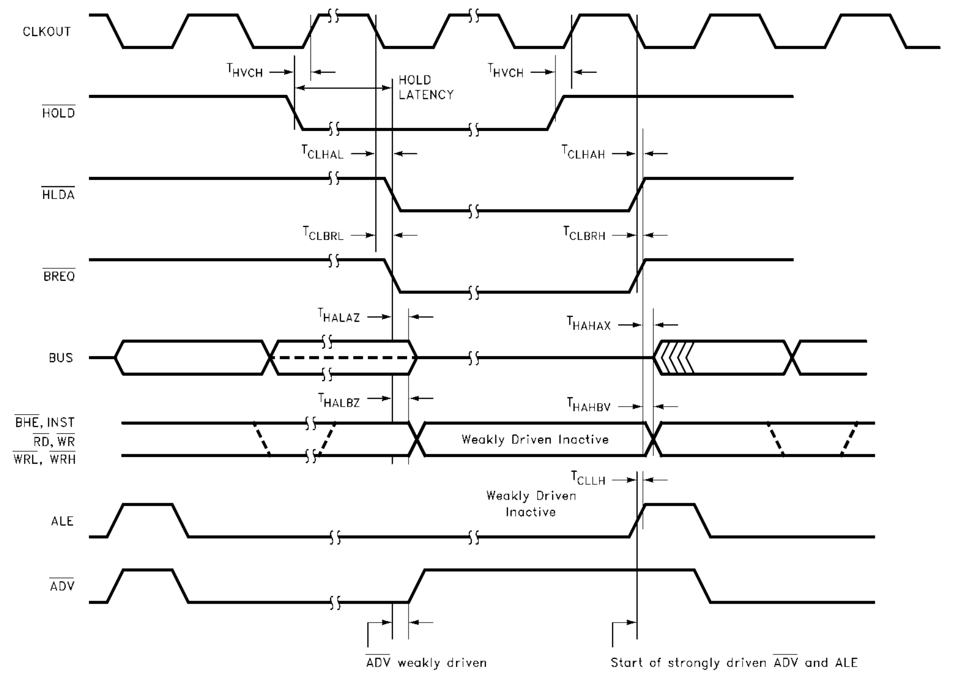
$\overline{HOLD}$/$\overline{HLDA}$ Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	$\overline{HOLD}$ Setup	+55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to $\overline{HLDA}$ Low	−15	+15	ns	
T_{CLBRL}	CLKOUT Low to $\overline{BREQ}$ Low	−15	+15	ns	
T_{HALAZ}	$\overline{HLDA}$ Low to Address Float		+15	ns	
T_{HALBZ}	$\overline{HLDA}$ Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+20	ns	
T_{CLHAH}	CLKOUT Low to $\overline{HLDA}$ High	−15	+15	ns	
T_{CLBRH}	CLKOUT Low to $\overline{BREQ}$ High	−15	+15	ns	
T_{HAHAX}	$\overline{HLDA}$ High to Address No Longer Float	−15		ns	
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10	+15	ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	+15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

Description	Min	Max	Units
Weak Pullups on $\overline{ADV}$, $\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{BHE}$	50K	250K	$V_{CC} = 5.5V$, $V_{IN} = 0.45V$
Weak Pulldowns on ALE, INST	10K	50K	$V_{CC} = 5.5V$, $V_{IN} = 2.4$



270942±36

Maximum Hold Latency

Bus Cycle Type	
Internal Execution	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

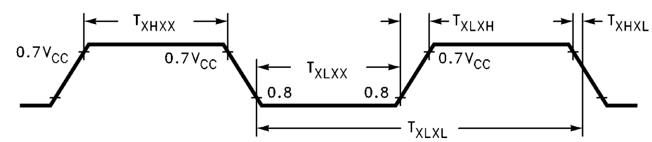
EXTERNAL CLOCK DRIVE (8XC196KC)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	20		ns
T_{XLXX}	Low Time	20		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE (8XC196KC20)

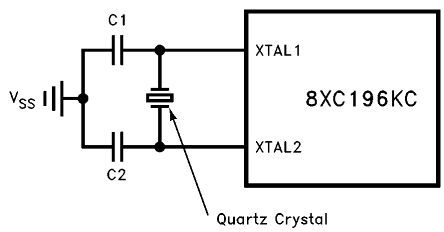
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	20.0	MHz
T_{XLXL}	Oscillator Period	50	125	ns
T_{XHXX}	High Time	17		ns
T_{XLXX}	Low Time	17		ns
T_{XLXH}	Rise Time		8	ns
T_{XHXL}	Fall Time		8	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270942–21

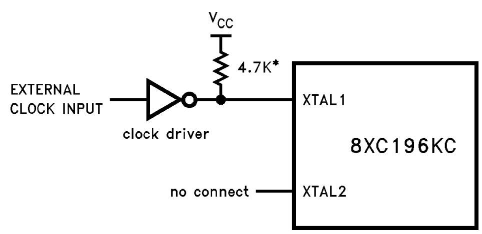
EXTERNAL CRYSTAL CONNECTIONS



270942–41

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = C2 ≈ 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

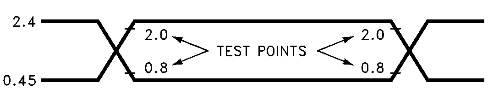
EXTERNAL CLOCK CONNECTIONS



270942–42

NOTE:
*Required if TTL driver used.
Not needed if CMOS driver is used.

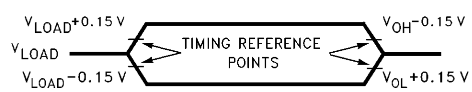
AC TESTING INPUT, OUTPUT WAVEFORMS



270942–22

AC Testing inputs are driven at 2.4V for a Logic ``1'' and 0.45V for a Logic ``0'' Timing measurements are made at 2.0V for a Logic ``1'' and 0.8V for a Logic ``0''.

FLOAT WAVEFORMS



270942–23

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs; $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by ``T'' for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:
- H- High
- L- Low
- V- Valid
- X- No Longer Valid
- Z- Floating

Signals:
- A- Address
- B- $\overline{\text{BHE}}$
- C- CLKOUT
- D- DATA
- G- Buswidth
- H- $\overline{\text{HOLD}}$
- HA- $\overline{\text{HLDA}}$
- L- ALE/$\overline{\text{ADV}}$
- BR- $\overline{\text{BREQ}}$
- R- $\overline{\text{RD}}$
- W- $\overline{\text{WR}}$/$\overline{\text{WRH}}$/$\overline{\text{WRL}}$
- X- XTAL1
- Y- READY
- Q- Data Out

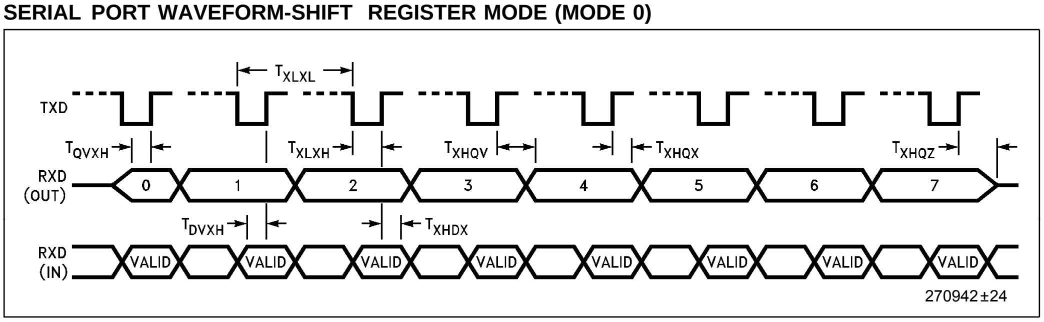
AC CHARACTERISTICS-SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING-SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM-SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT WAVEFORM-SHIFT REGISTER MODE (MODE 0)



A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Commercial Temp.	0	+70	°C
T_A	Ambient Temperature Extended Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	10	20	μs(1)
F_{OSC}	Oscillator Frequency (8XC196KC)	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency (8XC196KC20)	8.0	20.0	MHz

NOTE:
ANGND and V_{SS} should nominally be at the same potential, 0.00V.
1. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical (1)	Minimum	Maximum	Units	*Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1.0 ± 2.0	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 2
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An ``LSB'' as used here has a value of approxiimately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of all channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	7	20	μs(1)
F_{OSC}	Oscillator Frequency (**8XC196KC**)	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency (**8XC196KC20**)	8.0	20.0	MHz

NOTE:
ANGND and V_{SS} should nominally be at the same potential, 0.00V.
1. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		> −1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ωs	4
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An ``LSB'' as used here has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of all channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS DURING PROGRAMMING

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency During Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency During Run-Time Programming (8XC196KC)	6.0	16.0	MHz
F_{OSC}	Oscillator Frequency During Run-Time Programming (8XC196KC20)	6.0	20.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm. See user's manual for further information.

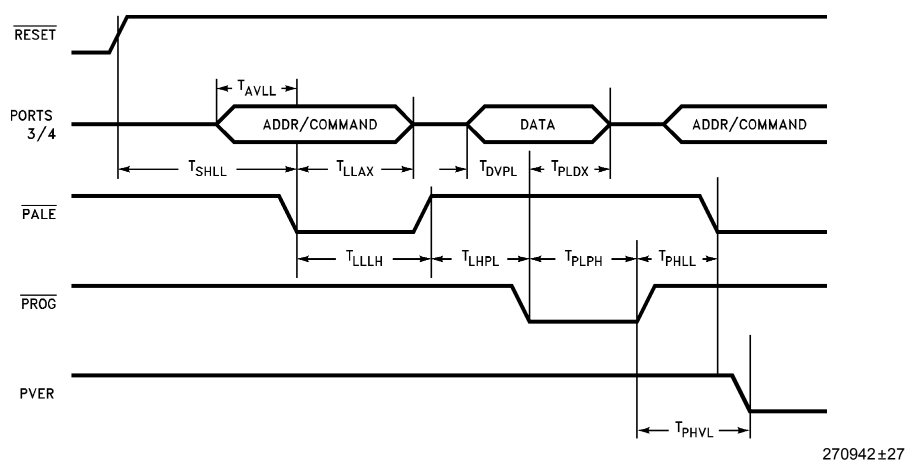
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

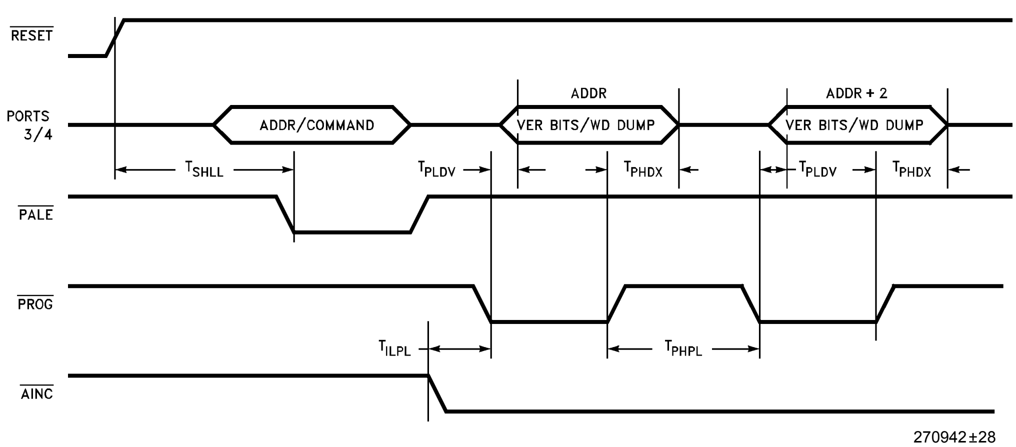
EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



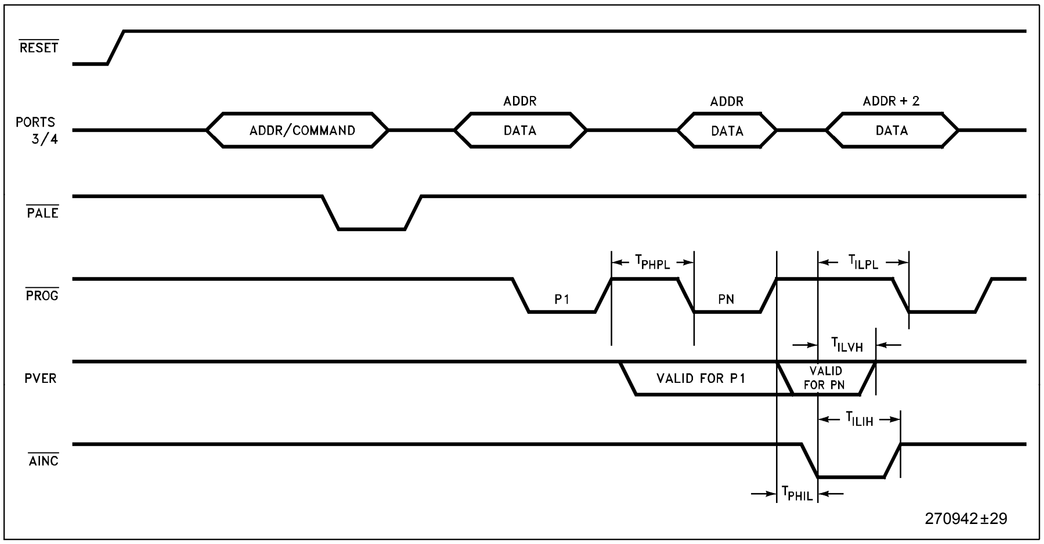
NOTE:
P3.0 must be high (``1'')

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low (``0'')

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



270942±29

8XC196KB TO 8XC196KC DESIGN CONSIDERATIONS

1. Memory Map. The 8XC196KC has 512 bytes of RAM/SFRs and an optional 16K of ROM/OTPROM. The extra 256 bytes of RAM will reside in locations 100H±1FFH and the extra 8K of ROM/OTPROM will reside in locations 4000H±5FFFH. These locations are external memory on the 8XC196KB.
2. The CDE pin on the KB has become a V_{SS} pin on the KC to support 16/20 MHz operation.
3. EPROM programming. The 8XC196KC has a different programming algorithm to support 16K of on-board memory. When performing Run-Time Programming, use the section of code in the 8XC196KC User's Guide.
4. ONCE Mode Entry. The ONCE mode is entered on the 8XC196KC by driving the TXD pin low on the rising edge of RESET. The TXD pin is held high by a pullup that is specified by I_{OH1}. This Pullup must not be overridden or the 8XC196KC will enter the ONCE mode.
5. During the bus HOLD state, the 8XC196KC weakly holds RD, WR, ALE, BHE and INST in their inactive states. The 8XC196KB only holds ALE in its inactive state.
6. A RESET pulse from the 8XC196KC is 16 states rather than 4 states as on the 8XC196KB (i.e., a watchdog timer overflow). This provides a longer RESET pulse for other devices in the system.

8XC196KC ERRATA

1. Missed EXTINT on P0.7.

   The 80C196KC20 could possibly miss an EXTINT on P0.7. See techbit MC0893.
2. HSI_MODEdivide-by-eight.
   See Faxback #2192.
3. IPD hump.

   See Faxback #2311.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a ``H'', ``L'' or ``M'' at the end of the topside tracking number. The topside tracking number consists of nine characters and is the second line on the top side of the device. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are differences between the 270942-006 datasheet and the 270942-005 datasheet:

1. Package prefix variables have changed. Variables are now indicated by an "x"

The following are differences between the 270942-004 and 270942-005 datasheets:

1. Removed ``Word Addressable Only'' from Port 3 and 4 in Table 2.
2. Renamed PVAL to CPVER.
3. Removed T_{LLYV} and T_{LLGV} from the waveform diagrams.
4. Added HSI_MODE divide-by-eight and IPD hump to 8XC196KC errata.

The following are important differences between the 270942-002 and 270942-004 data sheets:

1. NMI during PTS, QBD port glitch and Divide HOLD/READY erratas were fixed and have been removed from the data sheet. The HSI errata is also removed as this is now considered normal operation.
2. Combined 16 and 20 MHz data sheets. Data sheet 270924-001 (20 MHz) is now obsolete.
3. Added 80-lead SQFP package pinout.
4. Added documentation for CLKOUT disable bit.
5. θ_{JA} for QFP package was changed to 55°C/W from 42°C/W.
6. θ_{JC} for QFP package was changed to 16°C/W from TBD°C/W.
7. T_{SAM} (MIN) in 10-bit mode was changed to 1.0 μs from 3.0 μs.
8. T_{SAM} (MIN) in 8-bit mode was changed to 1.0 μs from 2.0 μs.
9. I_{IL1} specification for port 2.0 was renamed I_{IL2}.
10. I_{IL2} (MAX) is changed to TBD from $-$ 6 mA.
11. I_{IH1} (MAX) is changed to $+$200 μA from $+$100 μA.
12. I_{IH1} test condition changes to V_{IN} = 2.4V from V_{IN} = 5.5V.
13. V_{HYS} is changed to 300 mV from 150 mV.
14. I_{CC} (TYP) at 16 MHz is changed to 65 mA from 50 mA.
15. I_{CC} (MAX) at 16 MHz is changed to 75 mA from 70 mA.
16. I_{CC} (TYP) at 20 MHz is changed to 80 mA from 60 mA.
17. I_{CC} (MAX) at 20 MHz is changed to 92 mA from 86 mA.
18. I_{IDLE} (TYP) at 16 MHz is changed to 17 mA from 15 mA.
19. I_{IDLE} (MAX) at 16 MHz is changed to 25 mA from 30 mA.
20. I_{IDLE} (TYP) at 20 MHz is changed to 21 mA from 15 mA.
21. I_{IDLE} (MAX) at 20 MHz is changed to 30 mA from 35 mA.
22. I_{PD} (TYP) at 16 MHz is changed to 8 μA from 15 μA.
23. I_{PD} (MAX) at 16 MHz is changed to 15 μA from TBD.
24. I_{PD} (TYP) at 20 MHz is changed to 8 μA from 18 μA.
25. I_{PD} (MAX) at 20 MHz is changed to 15 μA from TBD.
26. T_{CLDV} (MAX) is changed to T_{OSC} $-$45 ns from T_{OSC} $-$ 50 ns.
27. T_{LLAX} (MIN) is changed to T_{OSC} $-$35 ns from T_{OSC} $-$ 40 ns.
28. T_{CHWH} (MIN) is changed to $-$5 ns from $-$10 ns.
29. T_{RHAX} (MIN) is changed to T_{OSC} $-$ 25 ns from T_{OSC} $-$ 30 ns.
30. T_{HALAZ} (MAX) is changed to $+$15 ns from $+$10 ns.
31. T_{HALBZ} (MAX) is changed to $+$20 ns from $+$15 ns.

32. T_{HAHBV} (MAX) is now specified at +15 ns, was formerly unspecified.
33. The T_{LLYV} and T_{LLGV} specifications were removed. These specifications are not required in high-speed systems designs.
34. Added EXTINT, P0.7 errata to Errata section.

The following are the important differences between the -001 and -002 versions of data sheet 270942.

1. Express and Commercial devices are combined into one data sheet. The Express only data sheet 270794-001 is obsolete.
2. Removed KB/KC feature set differences, pin definition table, and SFR locations and bitmaps.
3. Added programming pin function to package drawings and pin descriptions.
4. Changed absolute maximum temperature under bias from 0°C to +70°C to −55°C to +125°C.
5. Replaced V_{OH2} specification with I_{OH1} and I_{IL1} specifications.
6. Added I_{IH1} specification for NMI pulldown resistors.
7. Added maximum hold latency table.
8. Added external oscillator and external clock circuit drawings.
9. Changed Clock Drive T_{XHXX} and T_{XLXX} Min spec to 20 ns.
10. Fixed Serial Port T_{XLXH} specification.
11. Added 8- and 10-bit mode A/D operating conditions tables.
12. Specified operating range for sample and convert times.
13. Added specification for voltage on analog input pin.
14. Put operating conditions for EPROM programming into tabular format.